Claims 22-39 are pending in this application. Claims 27-39 are withdrawn from consideration. Claims 22 and 24 were rejected under 35 U.S.C. §102(b) as clearly anticipated by U.S. 5,357,125 to Kumagi. Claims 23 and 25 were rejected under 35 U.S.C. §103(a) as unpatentable over Kumagi. Claims 22 and 26 were rejected under the judicially created doctrine of obviousness-type double patenting as unpatentable over claim 11 of U.S. patent 5,751,024.

Addressing now the rejection of claims 22 and 24 under 35 U.S.C. §102(b) as clearly anticipated by Kumagi, and the rejection of claims 23 and 25 under 35 U.S.C. §103(a) as unpatentable over Kumagi, those rejections are traversed by the present response.

It is initially noted that claim 22 has been amended by the present response to clarify a structure therein. Specifically, claim 22 recites that the portion of the fourth semiconductor film that forms a channel region is the "only channel region of said insulated gate semiconductor device". According to that feature in the claimed invention, and with reference to Figure 14 in the present specification as only example, channel regions 53 are formed in the portion of the fourth semiconductor layer 44 that faces the control electrode 49 through the insulating film 48. Those are the only channel regions formed in the claimed invention. Such a feature in the claimed invention clearly distinguishes over the teachings in Kumagi.

More specifically, Kumagi expressly notes that in the device shown in Figure 4 therein "[a] channel region 66 is formed between the p^+ regions 65 extending in lateral direction, and the width of the channel region 66 is set at 3-10 μm, which is rather wide".[2]

[2]Kumagi at column 5, lines 5-8.

In such ways, it is clear that in Kumagi channel region 66 is formed, which is not provided in a portion of semiconductor layer 55, noted in the Office Action as corresponding to the claimed fourth semiconductor layer.

Further, in Kumagi a channel is formed not only in a region 66 sandwiched between p^+ regions 65 when a thyristor is in ON state, but also in a p layer 55 when a MOS transistor is in ON state. In Claim 22, on the contrary, a fourth semiconductor layer (e.g. 44) is the only channel region. Accordingly, Kumagi and Claim 22 of the present application are different.

OK

Moreover, Kumagi and Claim 22 of the present application are also different in that Kumagi combines an SI thyristor and an n-channel MOS transistor, whereas Claim 22 defines a structure of an IGBT. This is evident from the fact that Kumagi has channel forming regions in two different places, as mentioned above.

With respect to Claim 23, that claim further defines over Kumagi as Claim 23 defines a structure in which a second semiconductor layer 42 extends through a first semiconductor layer 41 and is partially exposed in a second main surface of the first semiconductor layer 41, as shown in Figure 23 as a non-limiting example. However, there is no disclosure in Kumagi of a structure in which second semiconductor layer 63 extends through a first semiconductor layer 61. Moreover, Claim 25 defines a structure in which a sixth semiconductor layer extends through a first semiconductor layer and is partially exposed in a second main surface of the first semiconductor layer, corresponding to Figure 22, for example. However, there is no disclosure in Kumagi of a structure in which a sixth semiconductor layer, even if n layer 62 is assumed to be the sixth semiconductor layer, extends through a first semiconductor layer 61.

OK

OK

OK

Thereby, the teachings in Kumagi do not meet the limitations of independent claim 22, and the claims dependent therefrom.

OK

In such ways, claims 22-25 patentably define over the teachings in Kumagi.

Addressing now the rejection of claims 22 and 26 under the judicially created doctrine of obviousness-type double patenting as unpatentable over claim 11 of U.S. 5,751,024, that rejection is also traversed by the present response.

U.S. patent 5,751,024 is a patent of the parent application of the present divisional application. Claim 22 of the present divisional application and Claim 11 of U.S. patent 5,751,024 are different in structure, since Claim 11 of U.S. patent 5,751,024 defines an IGBT having a trench gate, whereas Claim 22 of the present divisional application has been made assuming that an IGBT has a flat gate.

not OK

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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IN THE CLAIMS

--22. (Three Times Amended) An insulated gate semiconductor device, comprising:

a first semiconductor layer of a first conductivity type having first and second main surfaces on opposite sides thereof;

a second semiconductor layer of a second conductivity type provided on said first main surface of said first semiconductor layer;

a third semiconductor layer of said second conductivity type higher in an impurity concentration and thinner than said second semiconductor layer, and provided on a surface of said second semiconductor layer;

a fourth semiconductor layer of said first conductivity type provided on a surface of said third semiconductor layer, wherein said third semiconductor layer is interposed between said second semiconductor layer and a bottom of said fourth semiconductor layer and is in direct contact with said second semiconductor layer;

a fifth semiconductor layer of the second conductivity type selectively provided in a surface of said fourth semiconductor layer and opposing said third semiconductor layer through said fourth semiconductor layer;

a first main electrode disposed across and connected with surfaces of said fourth and fifth semiconductor layers;

a second main electrode provided on said second main surface of said first semiconductor layer;

an insulating film provided on a portion of said fourth semiconductor layer interposed between said third and fifth semiconductor layers; and

a control electrode facing said portion through said insulating film so that said portion forms a channel region as an only channel region of said insulated gate semiconductor device.--